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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,042	03/18/2004	Masaaki Ishida	250496US2	5628
22850	7590	07/18/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			LANE, JEFFREY D	
			ART UNIT	PAPER NUMBER
			2828	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/803,042	<b>Applicant(s)</b> ISHIDA ET AL.	
	<b>Examiner</b> Jeffrey D. Lane	<b>Art Unit</b> 2828	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 June 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 3/18/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/16/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### **Information Disclosure Statement**

1. The information disclosure statement filed 6/16/04 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a **column** that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

### **Specification**

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The disclosure is objected to because of the following informalities: Page 4 line 7 "...as close each other as possible" is grammatically incorrect.

Appropriate correction is required.

### **Claim Rejections - 35 USC § 102**

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 12-14, 23-28, 30, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kasai (US 6,246,705).

As for claim 1 Kasai discloses in figure 3, A laser modulating and driving device comprising: a modulation signal generating unit (modulator; See figure below) configured to generate a laser modulation signal consisting of a pair of small swing differential signals (133 and 132) based on pixel data (Imaging Data); and a driving unit (driver; See figure below) configured to drive a laser according to the laser modulation signal supplied from the modulation signal generating unit.

As for claim 23 Kasai discloses in figures 2 and 3, A laser modulating and driving device comprising: a pixel data generating unit 21 configured to produce pixel data and formed in a first block 200; a modulation signal generating unit 23 configured to generate a laser modulation signal from the pixel data and formed in the first block 20 together with the pixel data generating unit 21; a driving unit 11 configured to drive a laser according to the laser modulation signal supplied from the modulation signal

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generating unit and formed in a second block 100 spatially separate from the first block; and a signal transmission line 30 connecting between the first block 20 and the second block 10 and transmitting the laser modulation signal.

As for claim 30 Kasai discloses in figure 2, An image reproducing apparatus comprising: a photosensitive unit 5; a light source using a laser 2; a laser modulation signal generating unit 20 formed in a first block 200 and configured to produce a laser modulation signal consisting of a pair of small swing differential signals based on pixel data; a driving unit 10 formed in a second block 100 spatially separated from the first block and configured to drive the laser according to the laser modulation signal; a signal transmission line 30 connecting between the first block 200 and the second block 100 for transmitting the laser modulation signal to the driving unit 10; and a deflecting optical system 3 for guiding and deflecting a laser beam emitted from the light source 2 onto the photosensitive unit 5 to form a latent image thereon.

As for claim 12 Kasai discloses in figure 2, wherein the modulation signal generating unit and the driving unit are formed as spatially separated blocks 100 and 200, the laser modulating and driving device further comprising: a signal transmission line 30 for connecting the blocks to transmit the laser modulation signal from the modulation signal generating unit 20 to the driving unit 10.

As for claim 13 Kasai disclose in figure 3, a pixel data generating unit 21 configured to supply the pixel data to the modulation signal generating unit 23, wherein the pixel data generating unit 21 and the modulation signal generating unit 23 are formed on the same board 200.

As for claim 14 Kasai discloses in figure 3, a pixel data generating unit 21 configured to supply the pixel data to the modulation signal generating unit 23, wherein the pixel data generating unit 21 and the modulation signal generating unit 21 are formed as a single integrated circuit 20.

As for claim 24 and 31 Kasai discloses in figure2, wherein the first block and the second block are independent printed circuit boards (PCB).

As for claim 25 Kasai discloses in Figure 7, the modulation signal generating unit 23 has a small swing differential signal output circuit configured to output a pair of small swing differential signals as the laser modulation signal 23, the driving unit 11 has a small swing differential signal input circuit configured to receive said pair of small swing differential signals, and the signal transmission line (30, fig. 2) is configured to transmit said pair of small swing differential signals.

As for claims 26 and 27 Kasai discloses in fig. 4 and 5, the small swing differential signal output circuit has an output-stage circuit configured by a first logic (Pulse width signal, saturated or ECL), and the small swing differential signal (ramp output, unsaturated or CML) input circuit is configured by a second logic different from the first logic.

As for claim 28, Comparators and Op Amp's inherently have a pair of transistors. Therefore the limitations of the claims are met.

5. Claims 1-5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Ema et al. (US 5,946,334).

As for claim 1 Ema discloses, in figure 1, A laser modulating and driving device comprising: a modulation signal generating unit configured to generate a laser modulation signal consisting of a pair of small swing differential signals based (See Column 2 lines 58-63) on pixel data; and a driving unit configured to drive a laser according to the laser modulation signal  $I_{LD}$  supplied from the modulation signal generating unit. Differential signals may be caused by differences in current.

As for claim 2 Ema discloses, the modulation signal generating unit data has a modulation circuit configured to produce a modulation signal, and a small swing differential signal output circuit  $I_{LD}$  configured to convert the modulation signal to said pair of small swing differential signals, and the driving unit has a small swing differential signal input circuit for receiving said pair of small swing differential signals.

As for claim 3 Ema discloses in figure 20, a non-inverted fig. 20B and inverted fig. 20C signal generating circuit configured to produce a non-inverted signal fig. 20B having the same phase as the modulation signal fig. 20A and an inverted signal with the phase shifted by 180 degrees from the modulation signal; and a small swing output circuit configured to reduce swings of the non-inverted signal and the inverted signal to output said pair of small swing differential signals as the laser modulation signal.

As for claim 4 Ema discloses in fig 19a (See 42/47-48), the small swing output circuit is formed as current mode logic (CML) or emitter coupled logic (ECL) (271; See 41/37-40).

As for claim 5 Ema discloses in fig 19a, a reference potential of the CML or ECL is a supply voltage VCC of the modulation signal generating unit (the circuit 271 is connected to up to Vcc).

As for claim 7 Ema discloses in fig 19a, the small swing differential signal output circuit further includes swing reducing means arranged before the CML or ECL to decrease the swing of the non-inverted and inverted signals input to the CML or ECL (See 42/1-9).

6. Claims 1, 2, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hironari (JP H11-105336).

As for claim 1, Hironari discloses in drawing 1, A laser modulating and driving device comprising: a modulation signal generating unit (1 and 3) configured to generate a laser modulation signal consisting of a pair of small swing differential signals based on pixel data (See abstract); and a driving unit (2) configured to drive a laser LD according to the laser modulation signal supplied from the modulation signal generating unit.

As for claim 2, Hironari discloses, wherein the modulation signal generating unit has a modulation circuit configured to produce a modulation signal 1, and a small swing differential signal output circuit configured to convert the modulation signal to said pair of small swing differential signals 3, and the driving unit 2 has a small swing differential signal input circuit for receiving said pair of small swing differential signals. The circuit 3 would take turn the signal into differential circuits that are applied to it. See "Differential



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Amplifier" (<http://www.wikipedia.org>) for more inherent properties of the configuration of 3.

As for claim 16, Hinorari discloses, the modulation signal generating unit has an output-stage inverter or buffer having a ground terminal, to which a second voltage higher than a ground voltage is applied. Q3 (and Q4) create a voltage follower and I2 (and I3) create a current source. Q3 with I2 create a circuit that follows the voltage of the node (connected to Q2, R2 and Q3) without drawing significant power from the node, and therefore forms a buffer to output of the node. And therefore meets the limitations of the claim.

As for claim 18, Hinorari discloses, the modulation signal generating unit has an output-stage inverter or buffer using a transistor (Q3 and I2 or Q4 and I3), and wherein at least one of a high potential (Q3 or Q4) and a low potential (I2 or I3) that defines the a swing of said pair of small swing differential signals is generated by an ON resistance of the transistor

7. Claims 1-4, 6, 9, 15-17, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Thompson (US 5444728).

As for claim 1 Thompson discloses in figure 7, A laser modulating and driving device comprising: a modulation signal generating unit 32 configured to generate a laser modulation signal consisting of a pair of small swing differential signals (D1 and D2) based on pixel data (See abstract); and a driving unit (30 and 24) configured to

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drive a laser 12 according to the laser modulation signal supplied from the modulation signal generating unit.

As for claim 2, the modulation signal generating 32 unit has a modulation circuit configured to produce a modulation signal, and a small swing differential signal output circuit configured to convert the modulation signal to said pair of small swing differential signals D1 and D2, and the driving unit (30 and 24) has a small swing differential signal input circuit for receiving said pair of small swing differential signals (bases of 256).

As for claim 3, the small swing differential signal output circuit includes: a non-inverted and inverted signal generating circuit configured to produce a non-inverted signal having the same phase as the modulation signal and an inverted signal with the phase shifted by 180 degrees from the modulation signal (see column 13 lines 32-35); and a small swing output circuit configured to reduce swings of the non-inverted signal and the inverted signal to output said pair of small swing differential signals as the laser modulation signal.

As for claim 4, wherein the small swing output circuit is formed as current mode logic (CML) or emitter coupled logic (ECL); see column 13 lines 2-6. Note the claim requires the circuit to be ECL or CML not the output.

As for claim 6, a reference potential of the CML or ECL is an intermediate potential lower than a supply voltage VCC of the modulation signal-generating unit. There is current flowing through resistor 240 which would cause a drop in voltage from the supply voltage of +12V. Therefore the limitations of the claim are met.

As for claim 9 Thompson discloses, the small swing differential signal input circuit (30 and 24) has a differential signaling circuit using transistors.

As for claim 15, the modulation signal generating unit 32 has an output-stage inverter or buffer (236 or 232) having a supply terminal, to which a first voltage lower than a supply voltage (3.3 V) of the modulation signal generating unit is applied.

As for claim 16, the modulation signal generating unit 32 has an output-stage inverter or buffer (238 or 234) having a ground terminal, to which a second voltage higher than a ground voltage (3 V) is applied.

As for claim 17, the modulation signal generating unit has an output-stage inverter or buffer having a supply terminal (236, 232, 238, or 234), to which a first voltage lower (3.3 V) than a supply voltage of the modulation signal generating unit is applied (236 or 232), and a ground terminal (3V), to which a second voltage higher than a ground voltage is applied (238 or 234).

As for claim 20, Thompson discloses all that pertains to claim 1. Thompson further discloses, the modulation signal generating unit 32 is formed in a block spatially separated from the driving unit (30 and 24), and has an output-stage inverter or buffer (236 and 232 or 238 and 234) and a resistor 26 arranged outside the block to reduce a swing of an output of the output-stage inverter or buffer. The buffers 236, 232, 238 and 234 are commercially available chips (74F14 and DS0056) and therefore would have to be outside the block. Therefore all the limitations of the claim are met.

As for claim 21, Thompson discloses all that pertains to claim 1. Thompson further discloses, the modulation signal generating unit 32 has an output-stage inverter or buffer (232 and 236 or 234 and 238) and a resistor (252 or 254) connected to an output from the output-stage inverter or buffer (the resistor is connected to the buffer, therefore the limitation is met) to reduce a swing of the output from the output-stage inverter or buffer (intended use), and the driving unit (30 and 24) has an input-stage differential signaling circuit using a transistor 256.

### **Claim Rejections - 35 USC § 103**

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 22, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (US 6246705) in view of Kaminishi (US 6618406).

As for claims 22 and 29, Kasai discloses all that pertains to claims 1, and 25 respectively. However Kasai does not disclose that the input and output circuits of the small swing differential circuits use different supply voltages. Kaminishi discloses, "Since the control range of the DC bias current is large, here is used  $V_{cc}$  larger than  $V_{cs}$  as the power source of the amplifier. Furthermore... influences from changes and fluctuation in transistor characteristics and fluctuation in source voltage are

alleviated.”(Column 17 lines 25-34). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a larger Voltage (i.e. higher supply voltage) source for the driver (input) than the modulation circuit (output) to have a large control range. Also it would have been obvious because fluctuations in the source voltage are alleviated.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (US 5444728) in view of Kaminishi (US 6618406).

As for claim 8 Thompson discloses all that pertains to claims. However Thompson does not explicitly disclose that the input and output circuits of the small swing differential circuits use different supply voltages. Kaminishi discloses, “Since the control range of the DC bias current is large, here is used  $V_{cc}$  larger than  $V_{cs}$  as the power source of the amplifier. Furthermore... influences from changes and fluctuation in transistor characteristics and fluctuation in source voltage are alleviated.”(Column 17 lines 25-34). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a larger Voltage (i.e. higher supply voltage) source for the driver (input) than the modulation circuit (output) to have a large control range. Also it would have been obvious because fluctuations in the source voltage are alleviated.

11. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (US 5444728) in view of Trotter et al. (“A CMOS low voltage high performance interface” Trotter, J.D. Rekhi, S. Chava, V. Kale, P.C.; Microsyst.

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Prototyping Lab., Mississippi State Univ., MS, USA; ASIC Conference and Exhibit, 1994. Proceedings. Seventh Annual IEEE International ;19-23 Sept. 1994; pgs 44 – 48, Rochester, NY ).

As for claim 10 and 11, Thompson discloses all that pertains to claim 1.

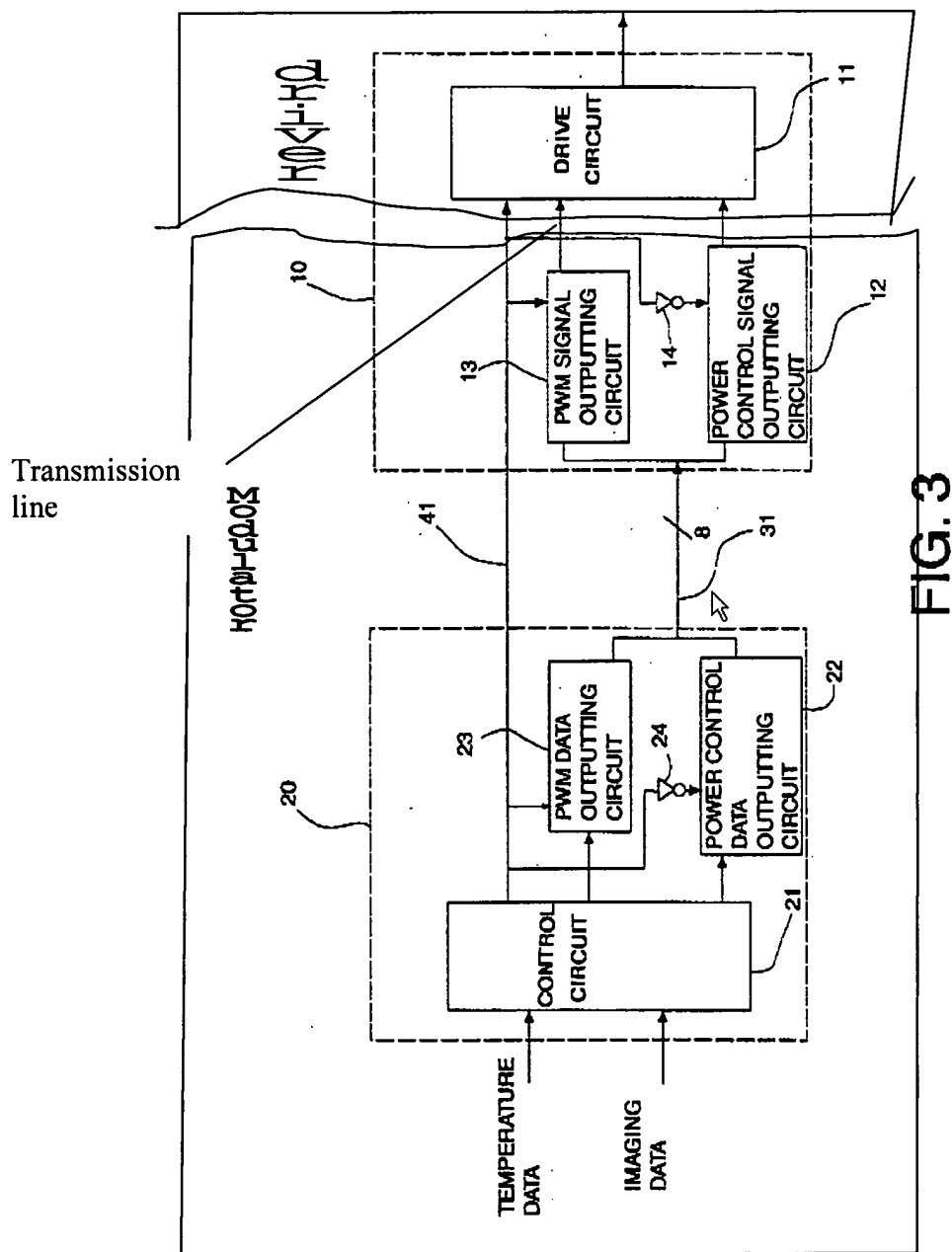
Thompson further discloses, a signal transmission line (D1 or D2) configured to connect the modulation signal generating unit 32 and the driving unit (30 and 24), through which said pair of small swing differential signals propagate (at D1 and D2). However Thompson does not disclose using parallel resistors at both ends of the transmission lines. Trotter discloses, "Parallel termination techniques with the voltage dividers (resistors) at each end of the bus matching characteristic impedance are preferred. In this case... there are no reflected waves (currents) and the initial signal is at full magnitude" (pg 47, second column 7<sup>th</sup>-3<sup>rd</sup> line from the bottom). Therefore it would have been obvious to terminate both end with resistors (voltage dividers) to prevent reflection of the voltage.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson (US 5444728) in view of Canright ("Practical design for controlled impedance" Canright, R.E., Jr. Martin Marietta Electron. Orlando, FL, USA; Electronic Components and Technology Conference, 1991. Proceedings. 41st: 11-16 May 1991; pgs. 370 – 377; Atlanta, GA).

As for claim 19, The laser modulating and driving device of claim 1, wherein the modulation signal generating unit has an output-stage inverter or buffer. However

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Thompson does not disclose a resistor in series with the buffer. Canright discloses "...even though the tolerance was allowed on the series termination resistor, the series termination produced a larger tolerance on  $Z_0$ ... Larger manufacturing tolerances are desirable" (pg 376 column 1 lines 2-7). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a series resistor on the transmission line, D1 and D2 (which is in series with the buffer), to allow for a larger tolerance.





### **Conclusion**

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kaminishi (US 6618406) discloses an optical communication laser driver with several claimed features.

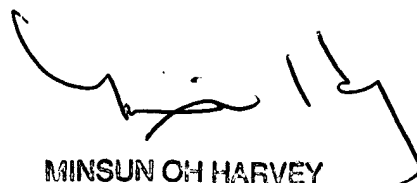
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey D. Lane whose telephone number is (571) 272-1676. The examiner can normally be reached on Monday thru Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey D Lane  
Examiner  
Art Unit 2828

JDL



**MINSUN OH HARVEY**  
**PRIMARY EXAMINER**